Special Feature: Power Semiconductor Devices

Research Report

Ultra-low Feedback Capacitance SiC JFET for High-frequency Operation

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ABSTRACT We propose a novel SiC vertical junction field-effect transistor (VJFET) with low feedback capacitance C_{rss}. A key feature of the proposed device is a p^+ screen grid inserted between the gate and drain electrodes, which is effective at reducing C_{rss} by 80% compared with a conventional VJFET. Due to the low C_{rss}, the proposed device has a faster switching speed and lower total power loss than any existing SiC transistor. We estimate that the carrier frequency of a DC/DC converter with the new type of VJFET can be increased more than two-fold compared to that with a trench gate MOSFET. Moreover, based on the low C_{rss}, we believe that the proposed device will enable high-frequency operation of power conversion systems and contribute to the miniaturization of power control units (PCUs) for HVs and EVs.

KEYWORDS Silicon Carbide (SiC), Power Semiconductor Devices, JFET, Feedback Capacitance, Switching Loss, Power Conversion System

1. Introduction

Power semiconductor switching devices are used in power conversion systems for the motor drive of hybrid electric vehicles (HVs) and electric vehicles (EVs). Currently, bipolar devices such as Si IGBTs and Si PiN diodes are mainly used as the switching devices. While minority carriers play an important role in reducing the on-state voltage drop in these Si bipolar power devices, they also contribute to the tail current and reverse recovery current to increase the switching loss. Therefore, there is a trade-off between the on-state voltage drop and switching loss. In order to resolve this issue, methods for carrier lifetime control, which introduce recombination centers by metal diffusion and charged particle beam irradiation,[1-3] have been investigated. Recently, because further improvement in the performance of Si bipolar power devices has been recognized as difficult, new technologies to overcome the limitations of Si materials are in high demand.

Silicon carbide (SiC) is a promising material for next generation power semiconductor devices because of its large critical breakdown electric field, high operating temperature and superior thermal conductivity. In particular, the large critical electric field makes it possible to increase the doping concentration and decrease the thickness of the voltage-sustaining layer (drift region) to maintain a breakdown voltage equivalent to that of conventional Si power devices. Therefore, even unipolar devices such as JFETs, MOSFETs and Schottky barrier diodes can achieve lower on-state voltage drop (on-resistance) in the case of SiC power devices. The switching loss of these devices is considerably low compared with Si IGBTs and Si PiN diodes because there is no tail current or reverse recovery current. A lower switching loss enables high-frequency operation of power conversion systems to keep the total power dissipation low and extends the driving range of HVs and EVs. High-frequency operation allows the miniaturization of power control units (PCUs) and in particular of passive components such as inductors and capacitors in the DC/DC converter (**Fig. 1**). Downsizing of the PCU is valuable because this provides greater flexibility for its installation and enables alternate layouts of a vehicle. We believe that SiC power devices will contribute to boosting the performance of HVs and EVs.

In this paper, we focus on the switching loss of SiC transistors that becomes apparent during high-frequency operation of power conversion systems and propose a novel SiC transistor that has lower switching loss.[4,5] In order to reduce the switching loss, it is necessary to rapidly switch between the on

and off states. High-speed switching can be achieved by reducing the feedback capacitance C_{rss}, which has to charge during the switching transient. We have therefore chosen to base our proposed low-C_{rss} transistor on SiC vertical JFETs (VJFETs) because they already have demonstrated low on-resistance[6-9] as well as no reliability or long-term stability concerns.[10,11] The proposed transistor adopts part of the structure of SiC buried gate static induction transistors (BGSITs),[8,9] a type of VJFET for which an extremely low on-resistance is easy to achieve.

2. Device Structure and Simulation

A schematic of the proposed VJFET, which we call a Screen Grid VJFET (SG-VJFET), is shown in **Fig. 2**. A major feature of the SG-VJFET is a p^+ screen grid, which is made of p-type SiC and is located between the buried p^+ gate and drain electrodes. This transistor usually operates with the screen grid electrode short-circuited to the source electrode. The screen grid weakens the capacitive coupling between the gate and drain to reduce C_{rss}. On the other hand, it also restricts the current flow to narrow regions, which increases the on-resistance. In order to suppress this effect, a current spreading layer, which is an n-type high impurity concentration layer, is introduced between the p^+ gate and screen grid.

To compare the performance of the SG-VJFET with that of other SiC FETs, device modeling of a trench VJFET (Tr. VJFET) and trench gate MOSFET (Tr. MOSFET) was carried out with a device simulator using published data.[6,7,12] The thickness and doping concentration of the voltage-sustaining layer (n^- drift layer) and n^+ substrate were made common among the three devices (n^- drift layer: 10 µm, 8×10^{15} cm^{-3}. n^+ substrate: 350 µm, 6×10^{18} cm^{-3}). For the SG-VJFET, the n^+ channel region was doped to slightly above 10^{16} cm^{-3} and the p^+ gate region was doped to 2×10^{19} cm^{-3}. For the Tr. MOSFET, we assumed an inversion channel mobility of 120 cm^2/V·s, which seems to be the best mobility currently available for this type of device.[13] A summary of the device structure and the static characteristics of the SiC FETs at room temperature are provided in **Table 1**.

To compare the dynamic characteristics of the SG-VJFET with that of the Tr. VJFET and Tr. MOSFET, a double-pulse clamped inductive load test was performed with test circuit shown in **Fig. 3**. The size of all transistors was the same (active area: 0.25 cm^2) to allow for comparison. A 650 VDC voltage was supplied to an inductor of 100 µH and a freewheeling SiC Schottky barrier diode (SiC SBD) with an active area of 0.25 cm^2. The total stray inductance L_s in the bus voltage path was set to 60 nH.

3. Results and Discussion

3. 1 Static Characteristics

The static characteristics of the SG-VJFET were calculated using the device simulator. The

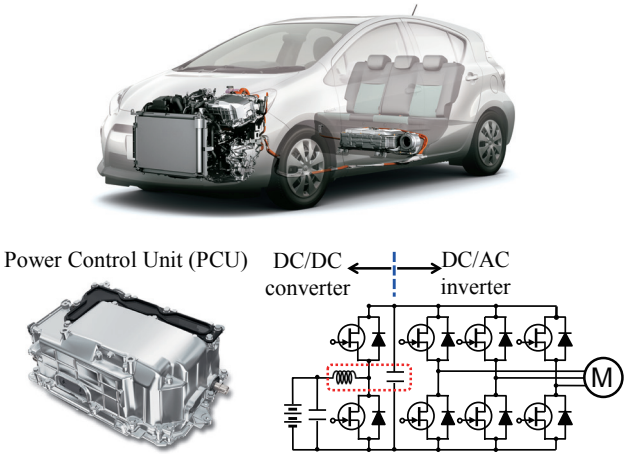


Fig. 1 Power conversion system for hybrid electric vehicles (HVs). Power control unit consists of DC/DC converters, DC/AC inverters, passive components and liquid cooling system.

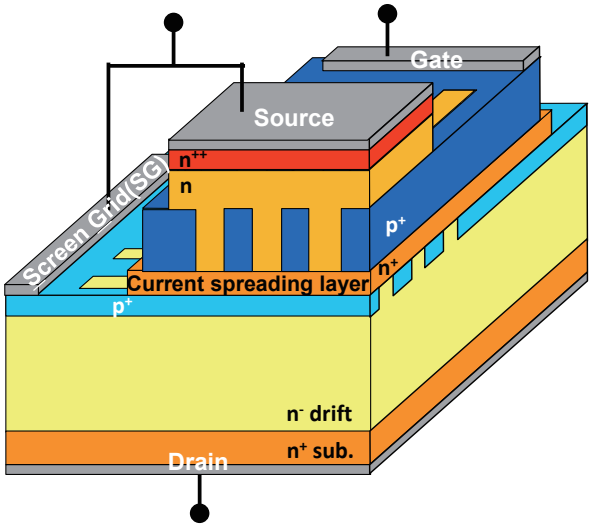
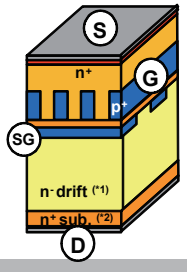
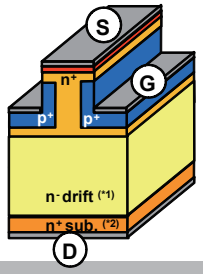
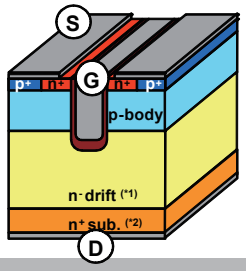


Fig. 2 A schematic diagram of the proposed SiC VJFET structure (Screen Grid vertical JFET: SG-VJFET).

Table 1 Summary of static characteristics for different types of SiC transistors.

	(Proposed device) SG-VJFET	Tr. VJFET	Tr. MOSFET
Device structure			
Specific on-resistance $R_{on}A$ @ V_{DS} = 1.0 V	2.4 mΩ·cm^2 (*3)	3.3 mΩ·cm^2 (*3)	2.7 mΩ·cm^2 (*4)
Threshold voltage V_{th} @ V_{DS} = 0.1 V, I_D = 0.1 A/cm^2	+ 1.0 V	+ 1.0 V	+ 6.1 V
Feedback capacitance C_{rss} @ V_{DS} = 650V	0.19 nF/cm^2	0.97 nF/cm^2	0.38 nF/cm^2

(*1) n$^-$ drift layer: 8×10^{15} cm^{-3}, 10 μm (*3) @ V_{GS} = 2.5 V
(*2) n$^+$ substrate: 6×10^{18} cm^{-3}, 350 μm (*4) @ V_{GS} = 15 V

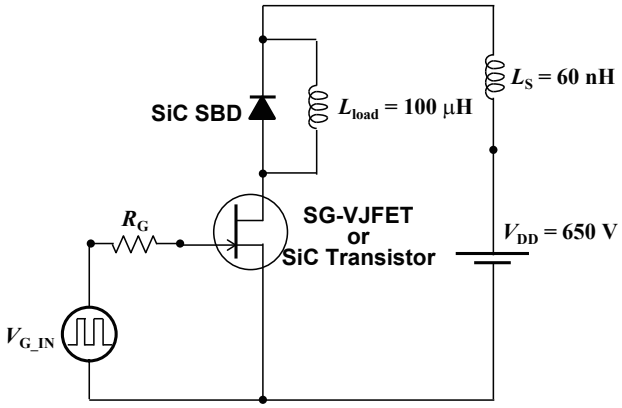


Fig. 3 Diagram of a standard inductive load test circuit to evaluate the dynamic characteristics of the three transistors.

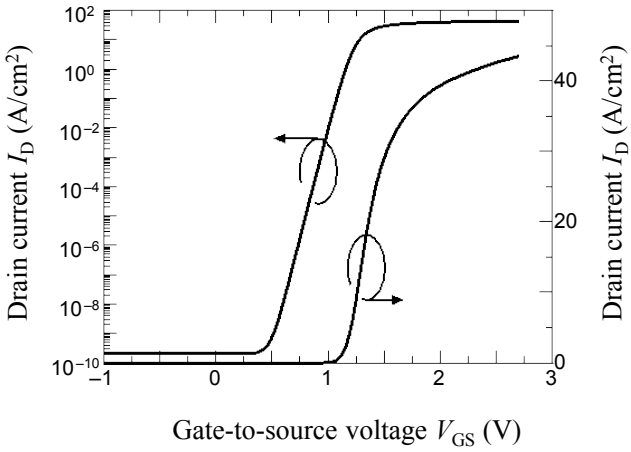


Fig. 4 Simulated transfer characteristic (I_D vs. V_{GS}) of SG-VJFET.

calculated transfer characteristic (I_D vs. V_{GS}) is shown in **Fig. 4**. A positive threshold voltage V_{th} of 1.0 V (@ V_{DS} = 0.1 V, I_D = 0.1 A/cm^2) was achieved, confirming the normally-off operation of the SG-VJFET. The calculated output characteristics (I_D vs. V_{DS}) are shown in **Fig. 5**. A specific on-resistance $R_{on}A$ (@ V_{GS} = 2.5 V, V_{DS} = 1.0 V) of 2.4 mΩ•cm^2 was achieved due to the fine line-and-space p$^+$ gate pattern. As shown in **Fig. 6**, a blocking voltage of more than 1500 V was achieved even at zero gate bias (i.e., V_{GS} = 0 V). **Figure 7** shows a comparison of C_{rss} for the three SiC transistors, which was smallest for the SG-VJFET and 80% lower than that of conventional VJFETs. It is therefore clear that the screen grid is effective at reducing C_{rss}.

3. 2 Dynamic Characteristics

To confirm the improvement in the dynamic characteristics of the SG-VJFET, a double-pulse test was performed on the three SiC transistors. The gate input voltage swing of the Tr. MOSFET

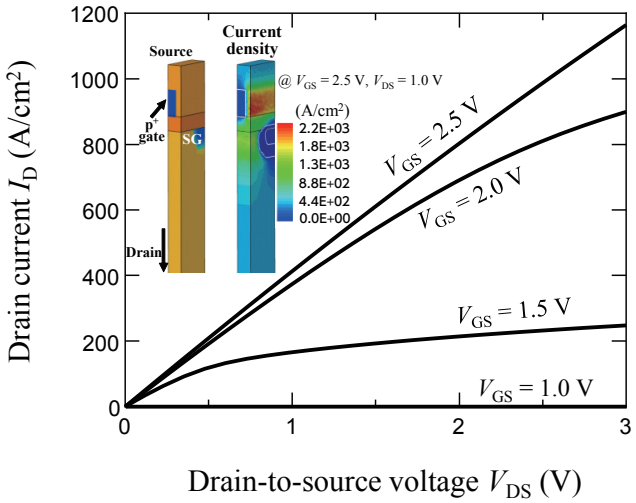


Fig. 5 Simulated output characteristic (I_D vs. V_{GS}) of SG-VJFET at V_{GS} = 1.0-2.5 V.

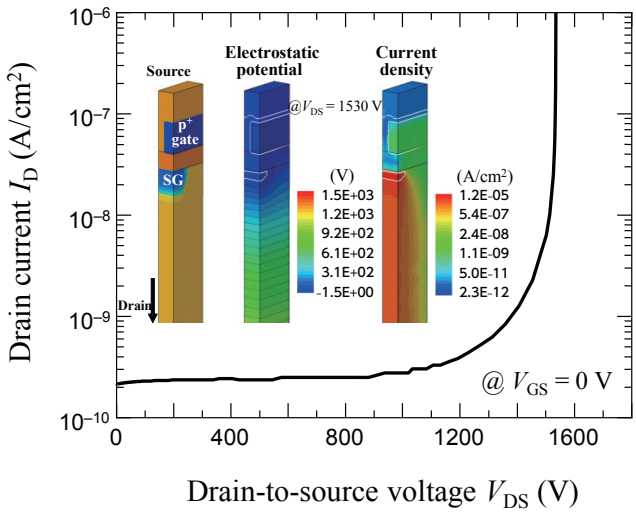


Fig. 6 Simulated forward blocking characteristic of SG-VJFET at V_{GS} = 0 V.

was $V_{G\_IN(off)}$ = 0 V to $V_{G\_IN(on)}$ = 15 V and that of both the SG-VJFET and Tr. VJFET was $V_{G\_IN(off)}$ = –5 V to $V_{G\_IN(on)}$ = 2.5 V. In order to easily evaluate the performance with only a comparison of the fall and rise rates dv/dt of the drain voltage V_{DS} during the turn-on and turn-off transient, the current rise and fall rates di/dt were adjusted to be the same for all three transistors.

The turn-on and turn-off waveforms at 650 V and 100 A are shown in **Figs. 8** and **9**, respectively. Due to the low C_{rss} of the SG-VJFET, its turn-on switching speed was the fastest among the three devices, as is apparent from Fig. 8. The turn-on switching loss E_{on}

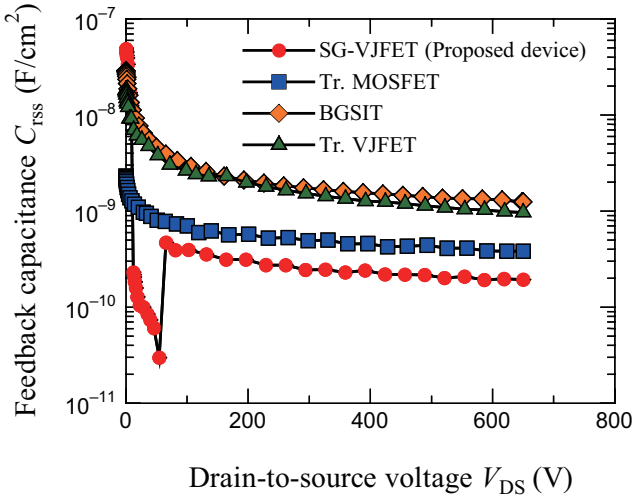


Fig. 7 Comparison of simulated feedback capacitance C_{rss} among three different types of SiC transistors.

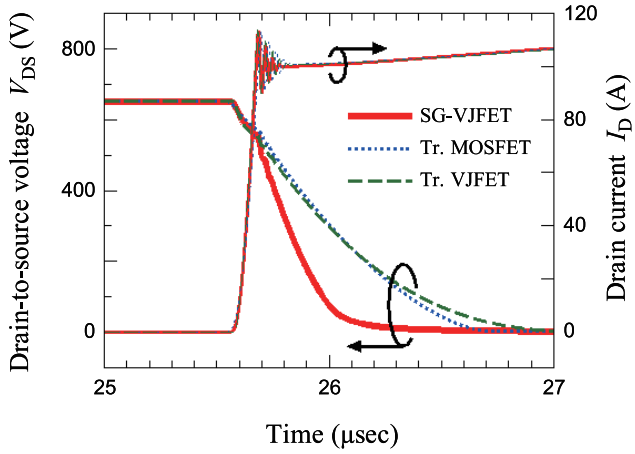


Fig. 8 Simulated turn-on switching waveforms of three different transistors. (V_{DD} = 650 V, I_D = 100 A)

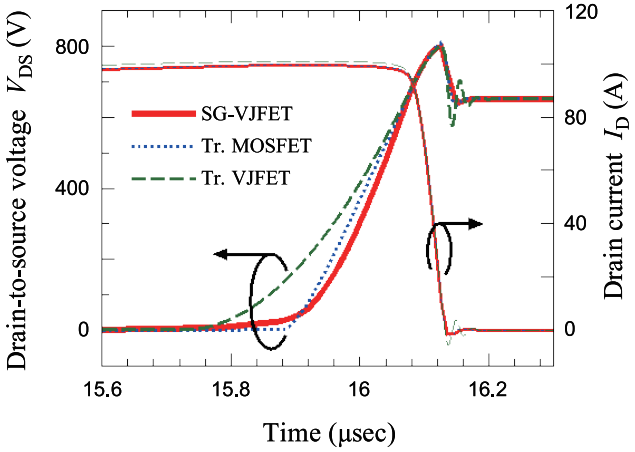


Fig. 9 Simulated turn-off switching waveforms of three different transistors. (V_{DD} = 650 V, I_D = 100 A)

was reduced by 50% and 60% compared with the Tr. MOSFET and Tr. VJFET, respectively. As shown in Fig. 9, the rise rates dv/dt of the SG-VJFET and Tr. MOSFET were roughly the same during the turn-off transient. The effect of reducing C_{rss} on the increase in dv/dt was small compared with the turn-on transient, and it is said that dv/dt typically depends on the gate-to-source capacitance C_{gs} during the turn-off transient.[14] Nevertheless, the turn-off switching speed of the SG-VJFET was the fastest among the three devices. The turn-off switching loss E_{off} of the SG-VJFET was 10% and 45% lower than that of the Tr. MOSFET and Tr. VJFET, respectively.

3. 3 Total Power Dissipation

The total power dissipation (the sum of E_{on}, E_{off} and the conduction loss E_{cond}) of each FET was estimated from the simulated static and dynamic characteristics, assuming that the converter carrier frequency and duty ratio were 10 kHz and 0.5, respectively. E_{on} and E_{off} were calculated under the same di/dt conditions (i.e., the same surge voltage ΔV_{surge}) taking into account noise due to electromagnetic interference and the breakdown voltage. The total power dissipation of the SG-VJFET was the lowest among existing SiC power devices (**Fig. 10**). Based on this estimation, the carrier frequency f_c of a DC/DC converter with an SG-VJFET can be increased more than two-fold compared with that using a Tr. MOSFET to maintain the same dissipation (**Fig. 11**). Based on these results, we believe that the SG-VJFET is suitable for fast switching applications.

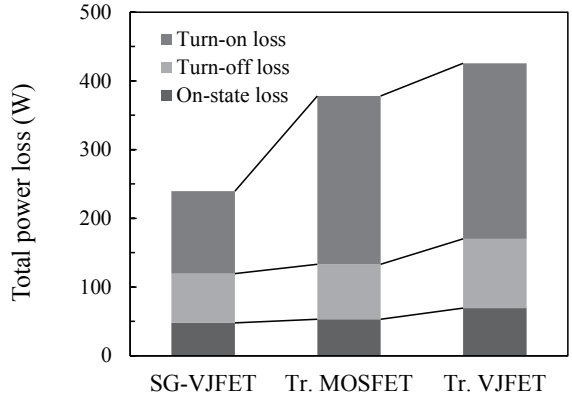


Fig. 10 Comparison of FET total power loss among three different transistors. (Switching current: 400 A/cm^2)

4. Conclusion

We propose a novel SiC VJFET with low feedback capacitance C_{rss} based on results obtained with a device simulator. A key feature of the proposed VJFET is a p^+ screen grid inserted between the gate and drain electrodes, which is effective at reducing C_{rss} by 80% compared with that of conventional VJFETs. Due to the low C_{rss}, the total power loss of the proposed SG-VJFET is lower than that for any existing SiC transistor. Based on these results, we believe this device will enable high-frequency operation of power conversion systems and contribute to the miniaturization of PCUs for HVs and EVs.

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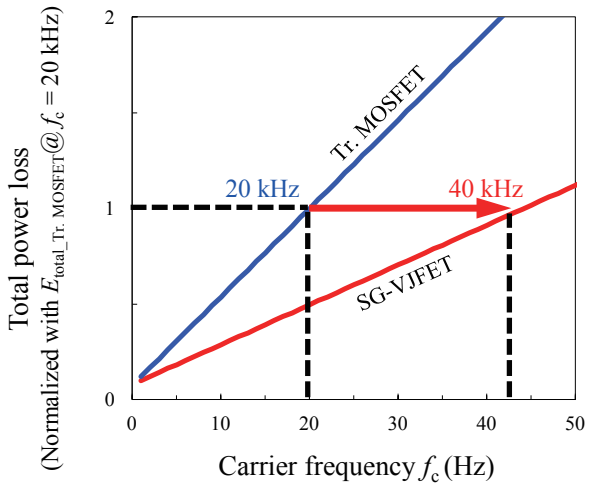

Fig. 11 Dependence of total power loss on carrier frequency f_c. Each data is normalized with total loss of trench-gate MOSFET at f_c = 20 kHz.

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Figs. 1, 2, 4-11 and Table 1
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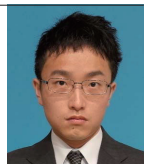

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